Gate Drive and Efficiency Analysis for a Silicon Carbide MOSFET Based Electric Motor Drive

Todd D. Batzel
Pennsylvania State University, Altoona College
tdb120@psu.edu

Taylor R. Leach
Pennsylvania State University, Altoona College
trl5162@psu.edu

Abstract

With increasing interest in vehicle electrification and renewable energy systems, the demand for improved power density and operating efficiency in energy conversion systems is intensifying. The recent wide-spread availability of Silicon Carbide (SiC) semiconductor switching components have offered potential for significant improvements to in energy conversion systems used for motor drives and inverters, and DC to DC converters,. SiC switching devices such as SiC MOSFETs and Schottky diodes are particularly attractive to developers of applications requiring compact, high efficiency energy conversion because of their low conduction and switching losses, their ability to operate at very high temperatures, and their high frequency switching capability as compared to Silicon-based MOSFETS and IGBTs.

Though SiC power electronic components offer great potential improvements in power conversion systems, fully realizing their benefits presents a challenge. SiC switches, due to their ultra fast switching speed are susceptible to transients introduced by rapid change in the drain-to-source voltage. Therefore, the gate drive requirements of SiC MOSFETS require a thorough analysis in order to prevent high *dv*/*dt* transients from causing erratic switching behavior or unnecessary switching loss. In addition, stray impedances can be the source of resonance during switching, which can lead to potentially destructive transient overshoots.

In this paper, a SiC based inverter used in motor drives is analyzed. The gate drive for a half bridge is developed, and trade-offs involving the optimization of power conversion efficiency within the operating condition limitations of the switching devices are analyzed by simulation. Switching and conduction losses are computed for the system and efficiency is determined. Finally, the overall impact of PWM switching frequency on the conversion efficiency is assessed.

Introduction

The power electronic switches used in commercial electric motor drives have, over the past several decades, been implemented using silicon-based semiconductor technologies, with

CMOS and IGBT devices dominating low voltage and high voltage applications, respectively [1]. The development and recent commercialization of Silicon Carbide (SiC) semiconductors has offered opportunities for significant improvements to electric motor drive systems, and there is a keen interest in integrating SiC based power switches into electric drives [2]. Though it is not yet a mature technology, SiC power switches promise to play an increasing role as a power switch used for motor drives in electric propulsion applications [3].

The advantages of SiC over Si-based semiconductors in power switching applications is mainly due to the lower on-state resistance and faster switching characteristics of SiC that can contribute to lower power losses in the switch itself [4]. SiC devices also have lower parasitic capacitances [5], operate at higher junction temperatures, and are easily paralleled for higher current applications [6]. These characteristics, if fully exploited, promise to improve the efficiency and power density of power conversion systems.

Several SiC electric motor drives for electric vehicle applications have already been developed and demonstrated. In [7], the efficiency of 3-phase inverters using SiC JFETs is compared through simulation with an IGBT based design in the output power range from 13 kW to 22 kW. The results show increasing efficiency improvements associated with the SiC design as the PWM frequency increases. Implementations of SiC based motor drives with output capability ranging from 11 kW up to 312 kVA are demonstrated in [6, 8-9]. Testing of these implementations confirm the benefits of using SiC power switches. The work in [10] discusses the importance of the gate-drive circuit design and consideration of parasitics in fully realizing the potential benefits of SiC power switches.

The purpose of this study is to develop and simulate the power electronics for a 12 kVA SiC MOSFET based half bridge that could be applied to electric propulsion system, for example. Performance of a 12 kVA half-bridge (1/3 of a 36 kVA three-phase inverter) is analyzed through component-level simulation. The gate drive for the SiC power switches is analyzed, and the switching behavior is optimized for minimal switching loss within the constraints of the device absolute maximum ratings. Overall conversion efficiency is characterized for various PWM switching frequencies, and opportunities for improved power density of the system are also considered.

Half-Bridge Converter

The half-bridge converter, as shown in Figure 1, is the basic building block for electric motor drives. Three of these paralleled half-bridge circuits sharing a common DC voltage source can be used to form a three-phase inverter that is capable of driving the motors used in electric propulsion applications - induction, synchronous reluctance, and permanent magnet synchronous machines.

The basic operation of the half-bridge converter shown in Figure 1 is now described. The electronic switches - SiC MOSFETs Sw1 and Sw2 in this case – are used to connect the DC source to the load. In the application of interest, the DC source is a battery with internal resistance R_{int}. The load in the application will be a three-phase permanent magnet

synchronous motor. Thus the load is inductive, and for purposes of analysis, it can be considered to be a constant current since the PWM switching period of the half-bridge is normally much shorter than the time constant of the motor phase winding. A gate driver, to be discussed later, is required for each switch. Free-wheeling diodes *D1* and *D2* are required in order to provide load current paths from source-to-drain.

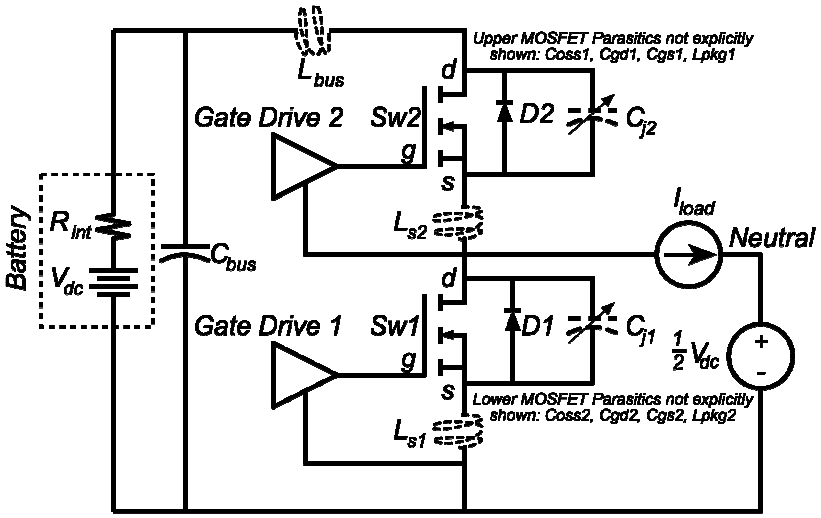


Figure 1. Half-Bridge, with parasitics shown in dashed lines

To turn on a SiC switch, a gate-to-source voltage exceeding the threshold of the device must be applied. Conversely, to turn off the switch, the gate driver applies a gate-to-source voltage well below the threshold.

In the half-bridge, only one of the two switches can be turned on at a time. Otherwise, damaging shoot-through current will flow from the DC source through the two switches, limited only by the source resistance and the on resistance of the switches. For positive load current (as shown in Fig. 1), when switch 2 is turned on (therefore switch 1 must be off) the current flow is from the DC source, through switch 2 and to the load. Conversely, when switch 1 is on (therefore switch 2 is off), the load current flows through the free-wheeling diode *D1* of the lower switch. If the load current is negative (opposite direction from current shown in Fig. 1) then the roles of switches 1 and 2 are reversed; with switch 1 is on, the load current flows through the lower MOSFET. Otherwise, load current will be through the free-wheeling diode *D2* of the upper switch. In a motor drive application the applied phase-to-neutral voltage is controlled by the duty cycle *D* of the switches through a PWM signal supplied by the controlling processor. The average phase-to-neutral voltage applied to the motor by the half bridge is given by:

$$V_{load} = V_{dc}\left(D - \frac{1}{2}\right). \tag{1}$$

The switching of the half bridge is now described, assuming a positive load current. Second order switching effects due to the parasitics shown in dashed lines in Figure 1 are analyzed in a later section. If the inverter is initially in a state such that both switches are off, the lower flyback diode *D1* is conducting the full load current, and the inductive load current is decaying. The upper switch *Sw2* is operating at zero current and the full DC bus voltage V_{dc} is across its drain-to-source connection. This corresponds to the point labeled *A* in the SiC MOSFET output characteristics shown in Figure 2, and actual switching waveforms in Figure 3. If the gate driver then turns the upper switch on, the gate-to-source voltage V_{gs} rises but V_{ds} of *Sw2* is clamped due to the lower diode *D1* conducting. As V_{gs} rises, the SiC MOSFET acts as a voltage controlled current source, and the switch begins to conduct current I_d. In Figure 2, this corresponds to movement from point *A* to point *B*. When the drain current I_d is equal to the load current, the lower diode can turn off, and V_{ds} of *Sw2* is no longer clamped. Thus, the operating point now moves horizontally from point *B* to *C*, as shown in Figures 2 and 3. At point *C*, the device on turned on, and operates in the ohmic region. At point *C*, the on resistance of the switch is rather low, and the product of the drain-to-source voltage and the drain current are called the conduction loss. Note also that higher gate-to-source voltages V_{gs} will yield lower conduction loss since they reduce the drain-to-source voltage, as shown in Figures 2 and 3.

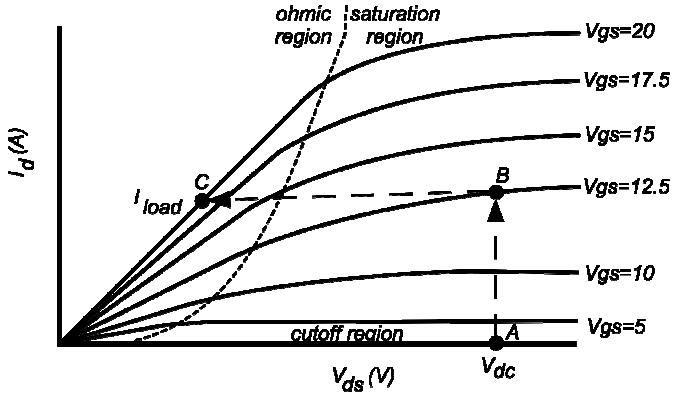


Figure 2. Power Switch Output Characteristics

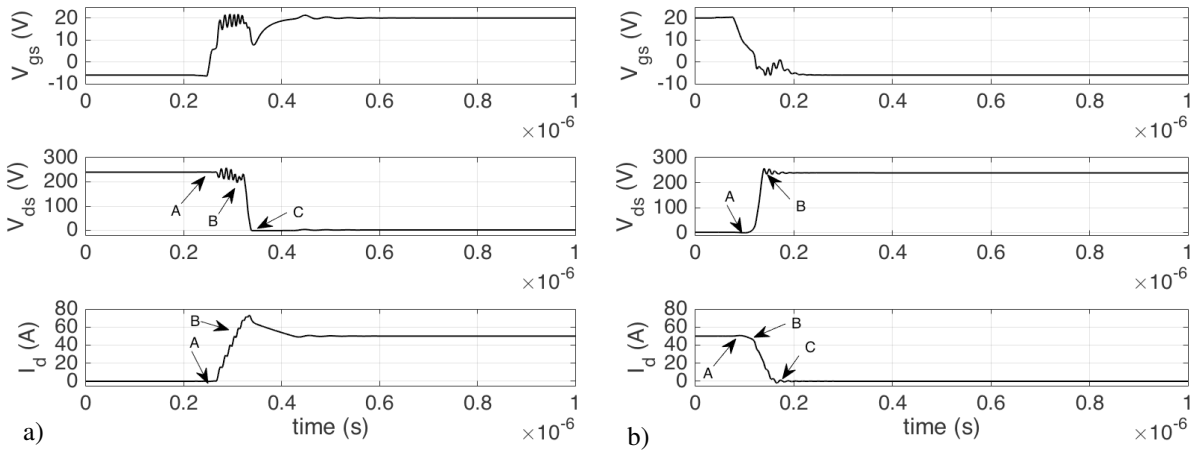


Figure 3. Waveforms for upper switch (a) turn on and (b) turn off with gate resistors of 5 Ω

A description of the upper switch turn-off for positive load current is quite similar. Initially, the upper switch *Sw2* is in the on state corresponding to operating point *C* in Figures 2 and 3. When the gate driver lowers the gate-to-source voltage for turn-off, the drain current is clamped due to the inductive load current. Thus, the operating point moves horizontally from *C* toward *B* in Figure 2, corresponding to an increasing V_{ds}. When operating point *B* is reached, the lower diode *D1* is able to begin conducting load current so that the *Sw2* current I_d can begin to decrease. The upper switch V_{ds} is now clamped by the lower diode, and the operating point moves from *B* toward *A* as the lower diode assumes more of the load current. At point *A*, the diode carries the full load current, and the upper switch is in the off state with the DC bus voltage across its drain and source.

As indicated above, when the upper switch is in the on state (point *C*), there is a conduction energy loss that is dependent on the drain-to-source voltage in the on state $V_{ds,on}$, the drain current, and the duty cycle *D* of the upper switch:

$$P_{con} = V_{ds,on} I_d D. \tag{2}$$

Likewise, each PWM cycle, the MOSFET is turned on and off and there is a corresponding switching energy loss E_{sw}. This switching loss can be determined by the path of the operating point as shown in Figure 2, and the corresponding switching transition times (the turn on and turn off times):

$$E_{sw} = \int_{turnon} V_{ds}(t) I_d(t)\, dt + \int_{turnoff} V_{ds}(t) I_d(t)\, dt\ . \tag{3}$$

The power loss due to switching P_{sw} depends on the PWM switching frequency f_{sw} :

$$P_{sw} = E_{sw} f_{sw} . \quad (4)$$

In the absence of a soft-switching scheme [11], these switching losses are unavoidable, but there are steps that can be taken to minimize them. These steps will be described in the next section.

Parasitics and Resonance in SiC MOSFET

The half-bridge circuit shown in Figure 1 includes several parasitic impedances indicated with the dashed lines. The connection of the DC bus has an associated inductance L_{bus}. Likewise, the connection between the gate driver and the source connection of the SiC MOSFET packages have an associated inductances of L_{s1} and L_{s2}, respectively, for the lower and upper switch. The flyback diode model, shown in Figure 4, includes a nonlinear junction capacitance - C_{j1} and C_{j2} for the lower and upper diodes, respectively. When the flyback diodes are forward biased, the junction capacitance is essentially short-circuited.

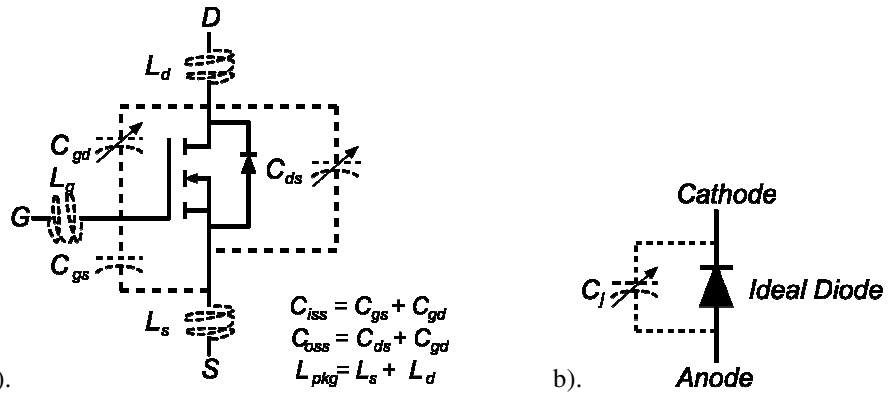


Figure 4. Circuit models including parasitics for a). SiC MOSFET and b). Schottky Diode

In addition to the half bridge parasitics shown in Figure 1, the SiC MOSFET also has parasitic impedances that must be considered for high device switching speeds. The SiC MOSFET model as shown in Figure 4 includes a gate-to-source capacitance C_{gs}, gate-to-drain capacitance C_{gd}, and a drain-to-source C_{ds} capacitance. Most data sheets specify total effective output capacitance C_{oss} and effective input capacitance C_{iss}. These effective values can be determined as indicated in Figure 4a. Some of these parasitic capacitances depend on the drain-to-source voltage, with highest capacitance occurring at low V_{ds}.

There are several ways in which the parasitics play an important role in the switching of SiC devices. One mode is the parasitics forming a resonant circuit in the power circuit that during switching transients can cause overshoots and ringing in the output voltage and current of the device. Another mode is the so-called Miller Effect [12] where the gate-to-drain capacitance forms a feedback loop such that a changing drain-to-source voltage can cause a plateau in the applied gate-to-source voltage, or in more severe cases can cause unintended turn on or turn

off of the switch. Yet another consideration is the formation of a resonant circuit in the gate drive circuit, and the interaction of the gate driver output impedance with the gate parasitic components.

To illustrate these parasitic effects, simulations were performed on the half bridge circuit. The switching waveforms shown in Figure 3 show a 125 MHz ringing at turn-on of the signals V_{ds} and I_d during the transition from operating point *A* to *B* of Figure 3a. This ringing is the result of the resonant circuit formed by the various parasitic components of the half-bridge at that operating condition. The parasitics in play are L_{bus}, C_{j2}, C_{oss2}, and L_{pkg2}. The lower half of the bridge is not critical for this state since the flyback diode *D1* is forward biased and the parasitics associated with the lower switch are short-circuited. An analysis of the circuit composed of the upper switch parasitics, upper flyback diode and its parasitics, as well as the DC voltage bus and its parasitic inductance shows that the resonant frequency is:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{\sqrt{\alpha+\beta} \pm \sqrt{\alpha-\beta}}{\beta}} \text{ , where} \tag{5}$$

$$\begin{aligned} \alpha &= C_{oss2}^2\left(L_{pkg2}+L_{bus}\right)^2 + L_{bus}^2 C_{j2}\left(C_{j2}+2C_{oss2}\right) \\ \beta &= 2C_{oss2}C_{j2}L_{bus}L_{pkg2} \end{aligned} \tag{6}$$

From the SiC MOSFET (Cree C2M0025120D) data sheets, $C_{oss2} = C_{j2}$=300 pf at a reverse bias voltage of 240V. The stray inductances used were L_{pkg2}=15 nH and L_{bus}=10nH. Using these component values with equations (5) and (6), the expected resonant frequency is 130 MHz, which agrees well with the 125 MHz resonant frequency shown in Figure 3.

After the lower diode turns off (between 0.4 and 0.5 μs in Figure 3a), the simulation shows a more subtle resonance at about 23 MHz. At this operating point, the parasitics associated with the lower switch will now impact the circuit, and the resonance is now due to the components L_{bus}, L_{pkg1}, C_{j1}, C_{j2}, C_{oss1}, and L_{pkg2}. The on state of the upper switch in this state makes the output capacitance C_{oss2} a non-contributor to the resonant circuit. A compact expression for the resonant frequency similar to equation (5) as a function of these components is not forthright, so the total impedance of the components contributing to the resonant circuit is plotted versus frequency in Figure 5 using C_{j2}=2500 pf (from Schottky diode data sheet – Cree CPW51200Z050B), $C_{j1} = C_{oss1}$=300 pf, and the same inductance values as noted previously. Note that there are several resonant frequencies associated with this circuit, the lowest of which is 23.1 MHz (145×10^6 r/s). This agrees well with the 23 MHz observed in Figure 3a.

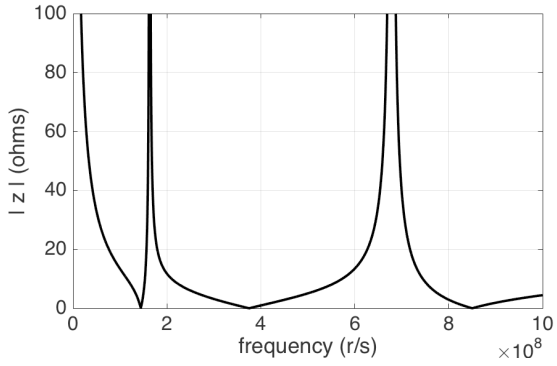


Fig. 5. Half-bridge Circuit Impedance with Upper Switch in the On State

The ringing and overshoot during switching is undesirable for several reasons. It can stress or damage components, and can be a contributor to radiated EMI [13]. Since it is not practical to insert resistance in the power circuit to overdamp the resonant circuit, other approaches must be considered. The addition of an external gate resistance can be used to slow the turn-on and turn-off times and therefore reduce the ringing and overshoot. This approach represents a trade-off between managing the overshoot and sacrificing some of the fast switching capability (and switching power loss) of the SiC device. This tradeoff will be discussed in more detail in the next section.

The other important characteristic of the switching waveforms in Figure 3 is the sudden dip in the gate-to-source voltage V_{gs} during the upper switch turn-on (at about 0.33 μs in Figure 3a, and the rise in V_{gs} during the turn-off (at about 0.15 μs in Figure 3b). Both of these deviations in the gate drive voltage during switching are due to the Miller Effect, where the gate-to-drain capacitance C_{gd} carries a current that charges or discharges the gate as V_{ds} changes. Furthermore, any change in the drain current I_d will result in a voltage across the stray source inductance (L_{s1} or L_{s2} as shown in Figure 1) that leads to a change in the effective V_{gs}. One way to reduce the Miller Effect coupling is to keep the output impedance of the gate driver low with high pulse current capability.

Note in Figure 3 that V_{gs} drops to about 7v during the turn on (Figure 3a), and rises to +1.5V after the turn off (Figure 3b). Although the drop to 7v is not enough to turn off the switch (the gate to source threshold voltage is approximately 2.5v), it will increase the on resistance and contribute to increased switching loss. The rise to +1.5v after turn-off could potentially turn the switch back to the on state since it is very close to the threshold (which is temperature dependent). If not addressed, these effects can lead to instability or unwanted, sporadic switching of the device [14]. This issue is addressed in the following section.

Gate Drive Design

The overall function of the gate driver is to supply the current required to rapidly charge and discharge the effective gate input capacitance (C_{iss}) to the required voltage level during turn on and turn off of the power switch, and to maintain the on or off state voltage levels during the switching transitions. It is typically recommended that SiC MOSFETs operate with a gate-to-source voltage of +20V for the on state, and -5V for the off state. Electrical isolation and level shifting are other functions of the gate driver.

Several SiC MOSFET characteristics require extra attention when designing the gate drive as compared to the needs of silicon-based power switch gate drivers (e.g. IGBT and Si MOSFET). The gate drive issues to be discussed in this section include the selection of gate-drive voltage levels and drive current, the rise and fall time limiting of the gate drive signal to mitigate ringing and overshoots as discussed in the previous section, and the gate driver impedance selection to alleviate the effects of crosstalk and the Miller capacitance – both of which can cause unintended switching or destructive voltage spikes in the half bridge. Each of these issues will place constraints on the gate driver design, and the end solution will address these constraints while minimizing switching and conduction loss. The gate driver implementation with the half bridge will then be simulated using LTSPICE to analyze the design.

The relatively low transconductance ($g_m = \Delta I_d / \Delta V_{gs}$) of the SiC MOSFET requires a rather large voltage swing of V_{gs} in order to optimize performance. Referring to the output characteristic of a typical SiC MOSFET shown in Figure 2, it is clear that large gate-to-source voltages (V_{gs}) yield the lowest on-state resistance that is necessary to minimize conduction losses. The switch is considered to be fully on when V_{gs} reaches about 17 v, and the lowest on-state resistance corresponds to V_{gs} of 20 v. No appreciable reduction in the on resistance is achieved by raising V_{gs} above 20 v. A typical SiC MOSFET begins to conduct at a minimum gate-to-source voltage threshold V_{th} of approximately 2.5V, so V_{gs} should be well below that threshold to assure that the switch operates in, and stays in, the off state. Therefore, it is often recommended to use a turn on voltage V_{gs} of +20V and turn off voltage of -5V for the SiC MOSFET. It should also be noted that the safe gate-to-source voltage range for the SiC MOSFET is between -10V to +25V, so any noise on V_{gs} that exceeds 5V can be potentially destructive if -5 and +20 volts are used at the gate-to-source levels.

To realize the fast switching capability of the SiC device and minimize the switching loss, the gate driver must be capable of sourcing and sinking a high peak current that is needed to quickly charge and discharge the gate capacitance to the required on and off state voltages. For the SiC MOSFET used in this study, the total gate capacitance (C_{iss}) is specified to be 2800 pf (or a bit higher when V_{gs} approaches zero) so that to charge and discharge the gate in 10ns requires a gate drive/sink current of

$$i_{gate} = \frac{C_{iss}\Delta V_{gs}}{\Delta t_{gc}} \ , \tag{7}$$

where ΔV_{gs} is the total gate to source voltage swing of 25V, and Δt_{gc} is the desired gate charge time of 10 ns. This yields a required gate current of 7A. This is implemented with a complementary N and P channel MOSFET pair (Si7465DP and Si7884DP) as shown in Figure 6, which also shows the connection to a half bridge circuit. The gate drive MOSFETs M1 and M2 discharge and charge, respectively, the gate of the lower SiC MOSFET. Likewise, M3 and M4 discharge and charge the gate of the upper SiC MOSFET in the half bridge. The turn-on and turn-off voltage levels are provided by +20V and -5V isolated DC-to-DC converters that must be referenced to the SiC MOSFET source connection.

As discussed in a previous section, the fast switching transitions that the SiC MOSFET is capable of make it necessary carefully manage the gate driver design, or significant ringing and overshoot can result. One method to reduce this effect is to add an external gate resistance to the gate charge and discharge current paths. This is shown in Figure 6, where *R1* and *R2* are the added gate resistance for the turn off and turn on of the lower SiC MOSFET. *R3* and *R4* are the added gate resistors for the upper SiC MOSFET driver. Separate resistances are used to better manage the turn on ($R_{g,on}$= *R2* and *R4*) and turn off ($R_{g,off}$=*R1* and *R3*) of the switch.

To demonstrate the effect of external gate resistance, consider the simulation shown in Figure 7, where no added gate resistance is used. With no added gate resistance, the upper switch drain current I_{d2} goes from its initial value to final value of 50A in approximately 30 ns. However, during turn on, there is an ac component on the drain current due to resonance, whose peak-to-peak amplitude is nearly 50A. Similarly, the drain to source voltage of the upper switch V_{ds2} has a peak-to-peak ripple of 150V. The resultant current overshoot is 40A. This level of overshoot and ringing is unacceptable, as it stresses components and leads to increased EMI emissions. The total switching loss energy for the upper switch (where the flyback diode is considered to be part of the switch) is obtained by integrating the instantaneous switch power P_2 shown in Figure 7 over the switching time interval, and is found to be 410 μJ for turn on, and 62 μJ for the turn off, for a total switching loss of 472 μJ per switching cycle. Note that the overshoots and ringing are not as prominent during the turn off of the upper switch because the gate drive signal has a gentler slope. This difference in slope is largely due to the gate capacitance being a function of V_{ds}, with the capacitance being significantly higher for low V_{ds}. This shows that slowing down the gate drive V_{gs} is useful for overshoot mitigation.

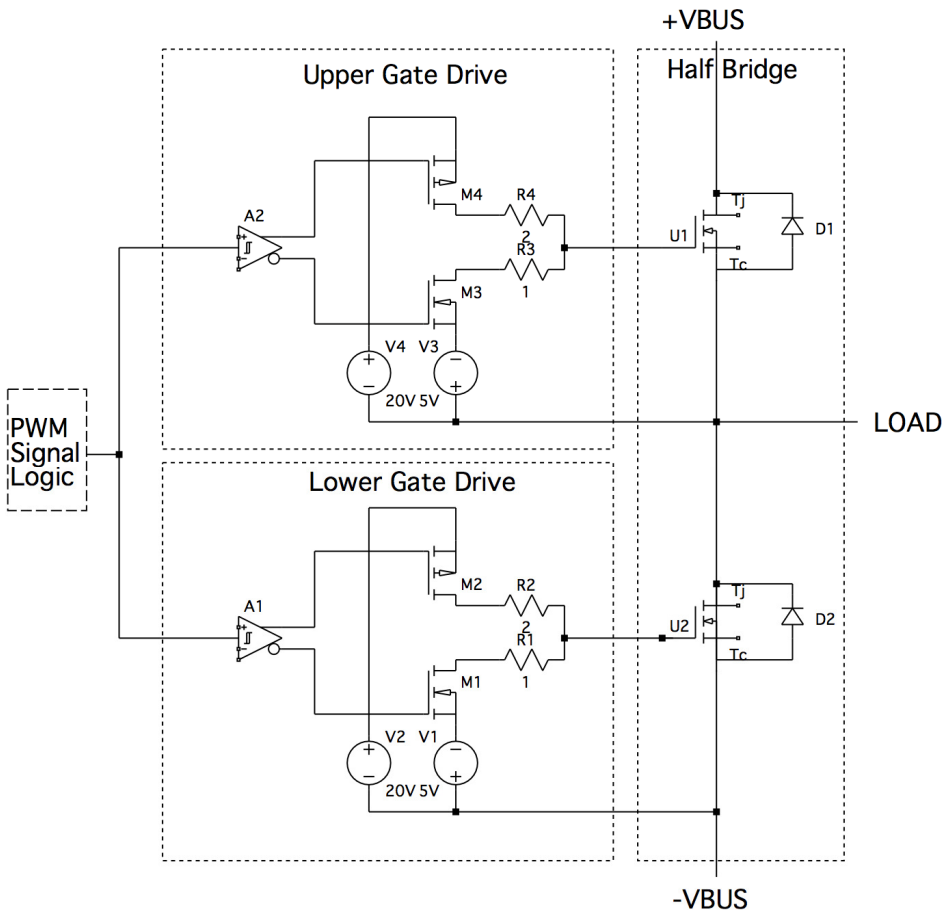
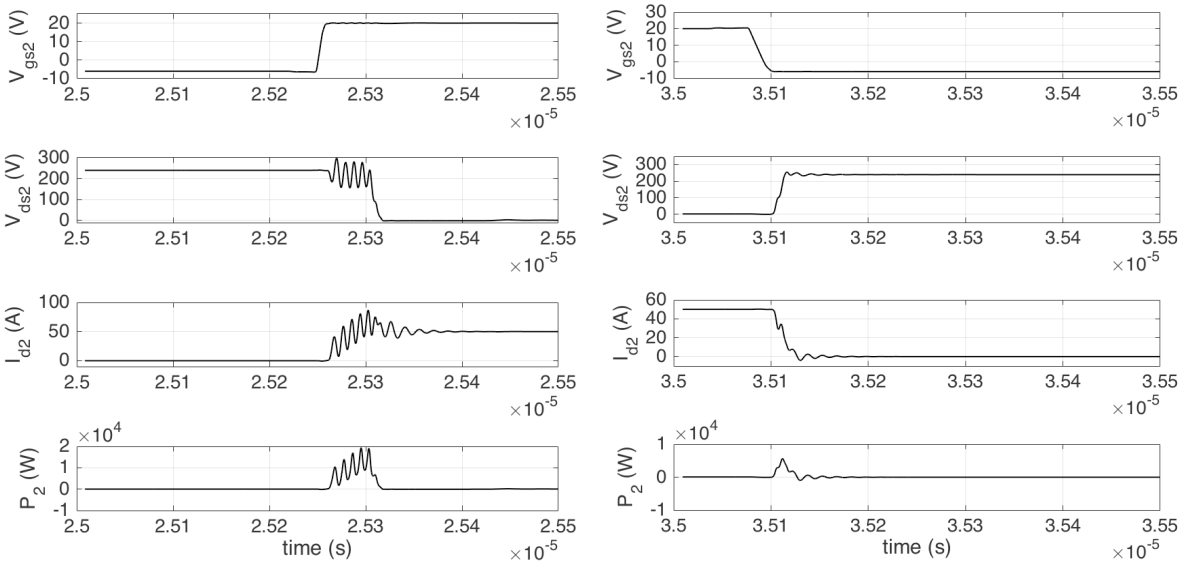


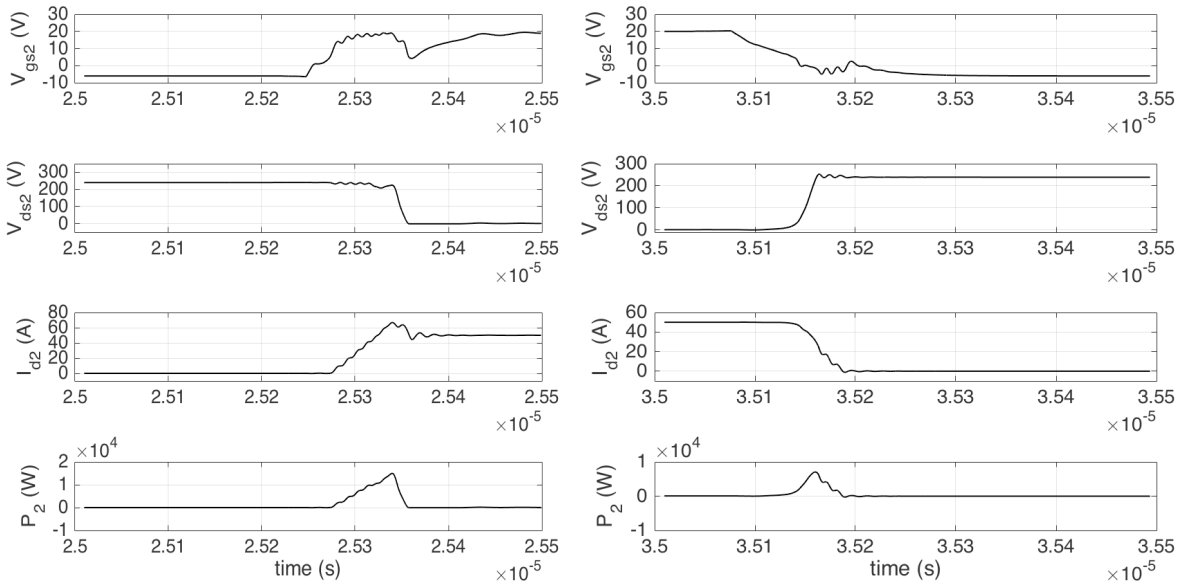
Figure 6. Gate Drive and SiC MOSFET Half Bridge



a). Upper Switch Turn-on b). Upper Switch Turn-off

Figure 7. Upper half-bridge switching waveforms - positive load current, 0 Ω in gate drive

To analyze the effect of increasing the gate resistance, the extra gate resistors (R1-R4 of Figure 6) are set to 10 ohms. The simulated switching waveforms are shown in Figure 8. As expected the gate drive voltage V_{gs} switching transition is much slower than the case with no added gate resistance. The result is significantly less ringing and overshoot in the drain current of the upper switch I_{d2} and its corresponding drain-to-source voltage V_{ds2}.



a). Upper Switch Turn-on b). Upper Switch Turn-off

Figure 8. Upper Half-bridge Switching Waveforms with $10\,\Omega$ in Gate Drive

This improvement in ringing obtained by adding external gate resistance, however, comes at a considerable expense. The total switching energy for the upper switch P_2 (flyback diode is considered to be part of the switch) obtained from the instantaneous power dissipation shown in Figure 8 is found to be 631 μJ for turn on, and 164 μJ for the turn off, for a total switching loss of 795 μJ per switching cycle. Thus, the switching loss has been increased significantly (by 68%) by the addition of the 10 ohm gate resistors.

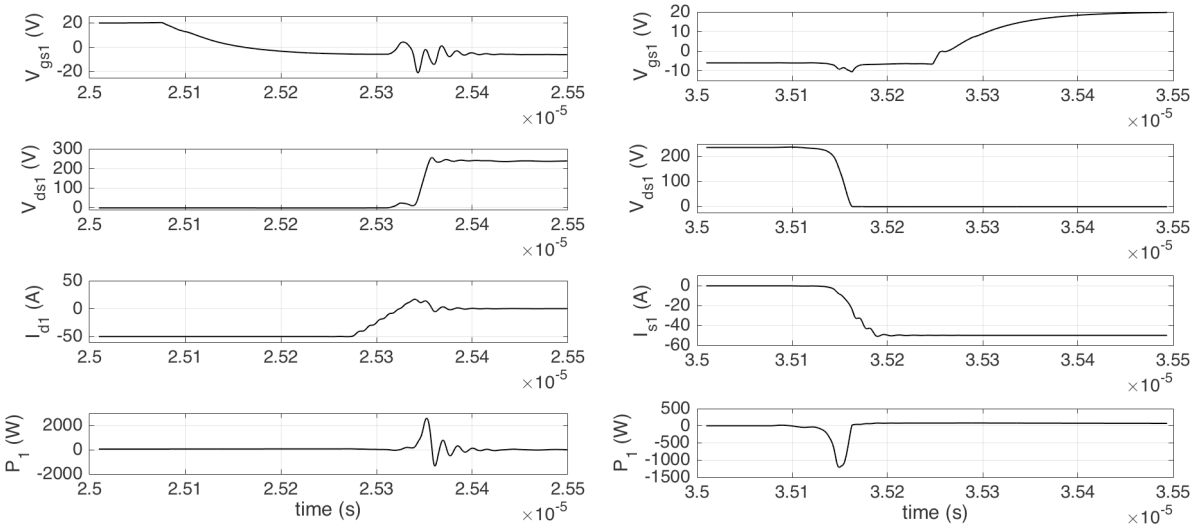
In addition to the increase in switching loss due the added gate resistance, there are now prominent deviations in the gate voltage V_{gs}. Figure 8a, for example, shows that during turn on, the gate voltage dips 2v, which is very close to the threshold voltage V_{th} of the device and therefore must be addressed. This sudden drop in the gate voltage could lead to unintentional turn off at worst, or at least unnecessary switching loss since the on state resistance is inversely proportional to the gate voltage. The cause of this drop in gate voltage is the sudden decrease in the drain voltage, which diverts current from the gate to the drain through the Miller capacitance C_{gd}. This current was also present in the case where no external gate resistance was added, but the effect was not prominent due to the low-

impedance of the gate driver. With the added 10 ohms in the gate drive, the currents in the parasitic Miller capacitance can lead to significant gate voltage drops, as shown in Fig. 8a. Another contributor to the drop in gate voltage is the sudden change in the upper switch drain current I_{d2}. This causes a change in the voltage across the stray source inductance L_{s2}, which couples even more current into the gate via the gate-to-source capacitance C_{gs}. These two phenomena are responsible for the significant drop in gate voltage in Figure 8a at approximately 2.535×10^{-5} s.

A similar situation arises during the turn-off of the upper switch, as shown in Figure 8b. During the turn-off, the gate voltage increases from its desired value of -5V to +2.5V. This is very close to the gate threshold voltage, and therefore could potentially turn the switch back on. The rise in gate voltage is due to the resonance in the circuit, a change of current in the stray source inductance, and the Miller coupling. Note, however, that parasitic coupling is not as severe as turn on since the applied V_{gs} has a lower slope for turn off.

Figure 9 shows what happens at the lower switch at the same time the upper switch turn on and turn off waveforms from Fig. 8 occur. For the positive load current used in the test, the lower half bridge is self-commutating since the flyback diode is carrying the load current. In Figure 9, note that there are spikes in V_{gs} that correspond to the upper switch transitions from Figure 8. This is called the crossover effect, where switching in the upper half bridge influences the lower half bridge signals and vice versa.

In Figure 9a, the gate signal of the lower SiC MOSFET switch is driven low, but since the flyback diode is carrying the positive load current, the gate signal has no effect on the state of the switch. Shortly after the lower switch gate is driven low, the upper switch gate is driven high (see Figure 8). When the upper switch in the half bridge starts to turn on, V_{ds} of the lower switch increases rapidly so that a current is driven from the drain to the gate through C_{gd}. This current must go through the gate resistor $R_{g,off}$ and the gate driver impedance into the -5V source. This causes a rise in V_{gs} to +4V, as shown in Figure 9a that starts to drive the lower switch mildly into the conducting state and initiates some unstable switching behavior. Due to resonance, the gate-to-source voltage V_{gs} of the lower switch reaches levels of -20V during this resonance at about 2.534×10^{-5} seconds. This is well below the maximum negative gate-to-source voltage of -10V, and could damage the SiC MOSFET.



a). Lower switch turn off b). Lower switch turn on

Figure 9. Lower Half-bridge Switching Waveforms with $10\,\Omega$ in gate drive

The crossover effect is also seen in Figure 9b. In this case, the upper SiC MOSFET is turned off at about 3.515×10^{-5} seconds, which causes a drop in V_{ds} across the lower switch so that a current flows from the lower switch gate to drain through C_{gd}. This current flows through the external gate resistance $R_{g,off}$ so that the gate voltage V_{gs} drops below -5V. The crossover coupling is not as pronounced in Figure 9b since *dv/dt* of the drain-to-source voltage is comparatively low. Regardless, it is clear that the selection of the gate resistance is important in reducing the effects of crosstalk as well as overshoots and ringing.

Gate Drive Resistance Selection

Using no additional external gate resistance gives the fastest possible switching transitions and thus very low switching losses. However, as shown in Figure 7, the very fast switching can also yield excessive ringing and overshoot. To mitigate the overshoot, external gate resistance can be added to slow down the switching, but this increases the switching loss, and the added gate drive impedance can lead to stability issues or operation of the SiC MOSFET outside of its rated V_{gs} operating range of -10V to +25V. The choice of gate drive resistors, therefore, represents an engineering tradeoff and must be carefully assessed.

Component level circuit simulations were performed using LTSPICE for various combinations of gate resistance, and the switching losses were computed. The results are summarized in Figure 10, which confirms that switching losses increase with the external gate resistance. Specifically, the addition of gate resistance $R_{g,on}$ increases the turn-on switching loss, while adding $R_{g,off}$ increases turn-off switching loss. Figure 11 shows the total switching loss per switching cycle as a function of the selected gate resistance.

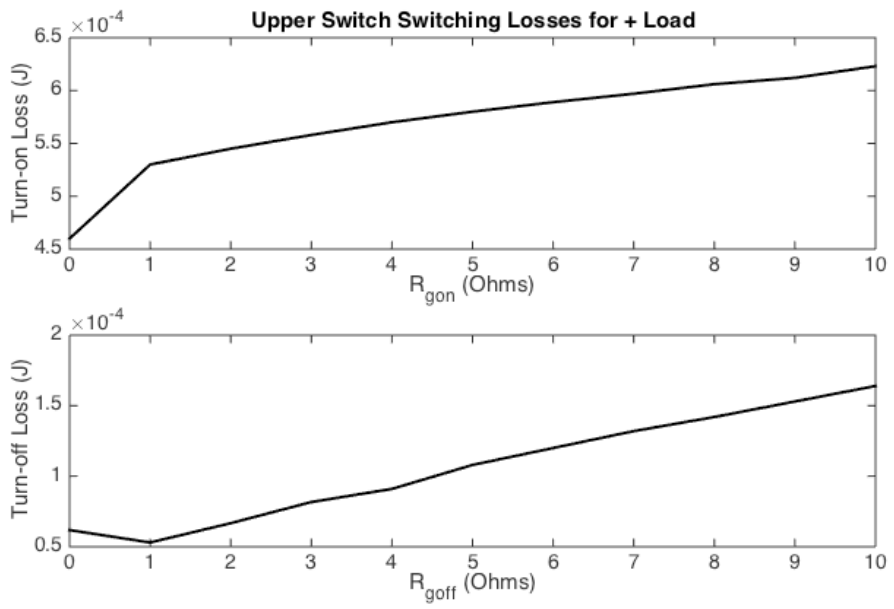


Figure 10. Turn On and Turn Off Loss Versus External Gate Resistance

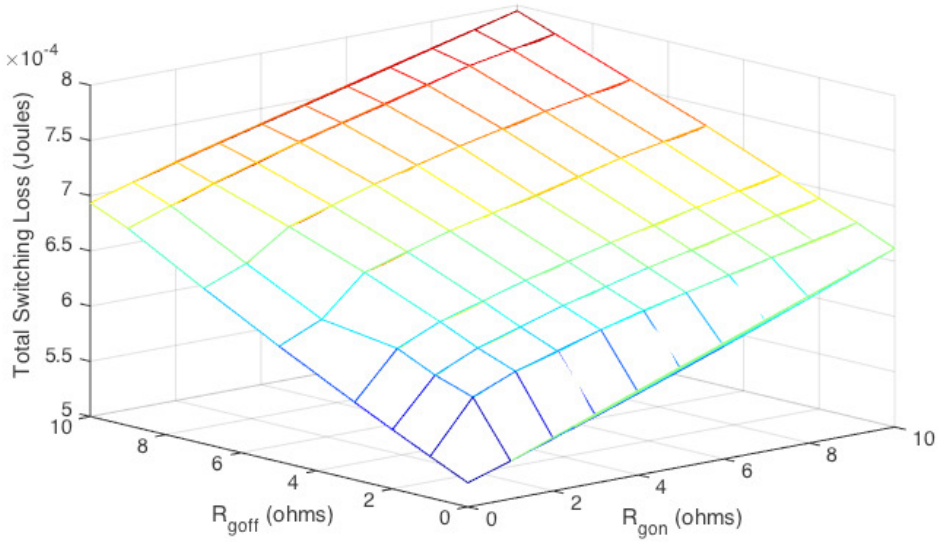
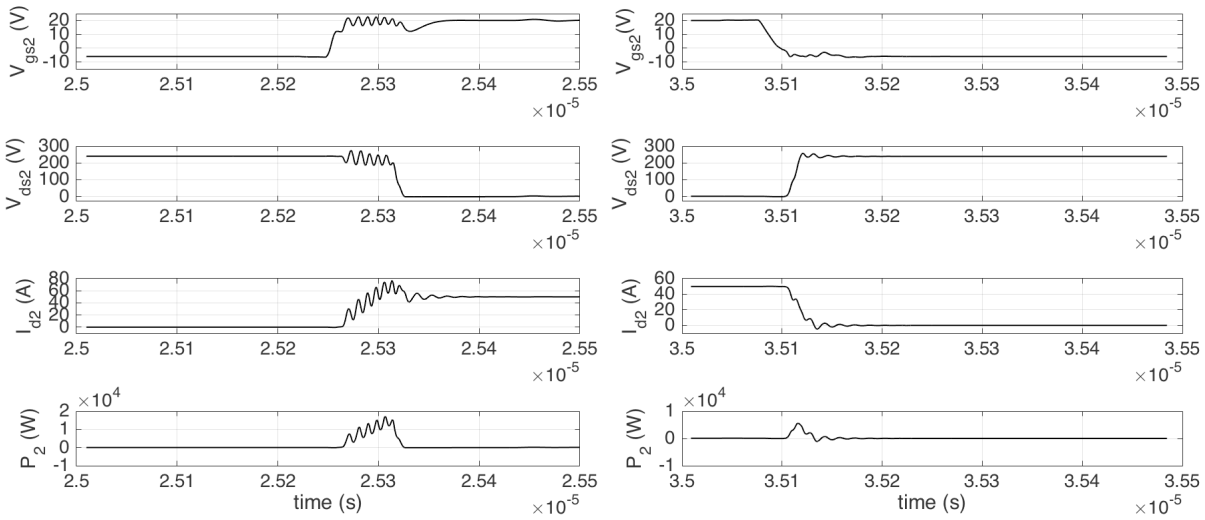


Figure 11. Total Switching Loss per Cycle for Various External Gate Resistor Values

The simulation results were also analyzed to see the correspondence between gate resistance values and the V_{gs} excursions that may violate device ratings. The simulations reveal that for positive load current, higher $R_{g,on}$ leads to more severe dips in the upper switch V_{gs} during turn on, while larger $R_{g,off}$ tends to create higher surges in upper switch V_{gs} while the device is being driven off. Due to crosstalk, the lower switch deviations for positive load current depend largely on the slope of the upper switch V_{ds}. For negative load current, the roles are

reversed. That is, the lower switch gate resistances determine deviations in the lower switch V_{gs}, while the upper switch V_{gs} deviations are due to crosstalk from the lower gate transitions. In general, the results showed that any combination of $R_{g,on} \leq 2\Omega$ and $R_{g,off} \leq 1\Omega$ led to gate-to-source voltages that were safely within the device ratings, with no danger of inadvertent turn-on or turn-off of the device. Based on this analysis, the values $R_{g,on} = 2\Omega$ and $R_{g,off} = 1\Omega$ were selected as a compromise between minimizing switching loss, maintaining the device within its safe operating range, and avoiding excessive overshoots and ringing. Figures 12 and 13 show the switching transitions of the upper and lower switches, respectively, for this selection of gate resistance.

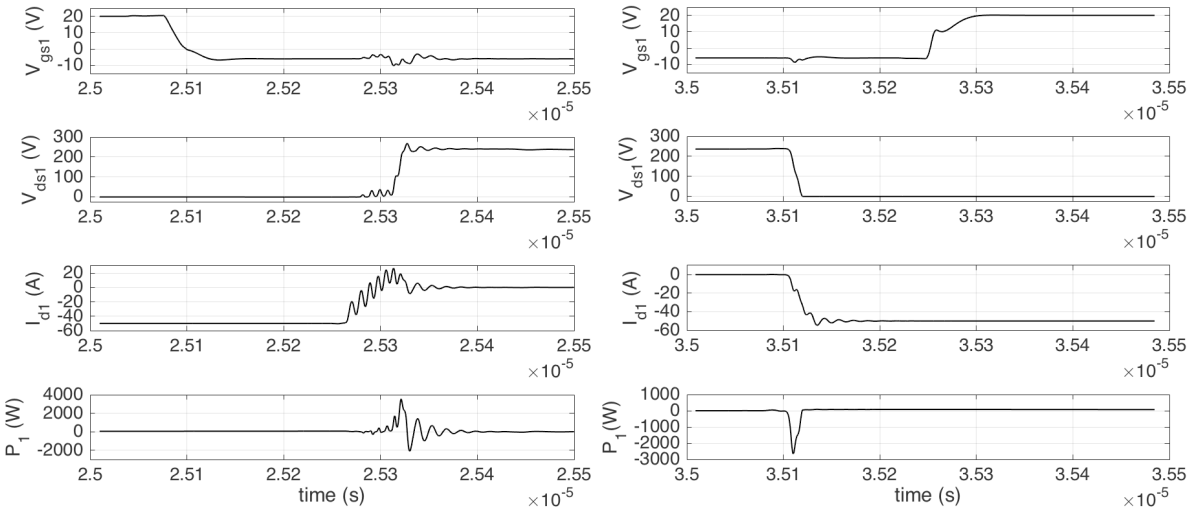


a) upper switch turn on b). upper switch turn off

Figure 12. Upper Switching Transitions for $R_{g,on} = 2\Omega$ and $R_{g,off} = 1\Omega$

Analysis of Switching and Conduction Losses in the Half-Bridge

Using the selected gate resistor combinations from the previous section, the switching and conduction losses are now analyzed for a range of load current up to 50A, which is the rated maximum continuous current for the SiC MOSFET used in the study. The simulations assume operation at a case temperature of 25 degrees C. The results are compiled in Table 1.



a) lower switch turn off b). lower switch turn on

Figure 13. Lower Switching Transitions for $R_{g,on} = 2\Omega$ and $R_{g,off} = 1\Omega$

Table 1. Switching Loss for Positive Load Current

	I_{load}=50 A	I_{load}=40A	I_{load}=30A	I_{load}=20A	I_{load}=10A
Upper turn on	547 μJ	380 μJ	258 μJ	150 μJ	76.2 μJ
Lower turn off	23.7 μJ	25.4 μJ	24.6 μJ	24.2 μJ	25.4 μJ
Upper turn off	53.1 μJ	40.6 μJ	23.7 μJ	21.7 μJ	22.4 μJ
Lower turn on	-19 μJ	-19.7 μJ	-20.5 μJ	-21.7 μJ	-22.6 μJ
Total W_{sw}	604.8 μJ	426.3 μJ	285.8 μJ	164.2 μJ	101.4 μJ

Note that the switching losses for the upper switch are approximately proportional to the load current level, as expected, while the lower switching loss is not. Also, the results of the table can be used for negative load current as well, by translating the upper and lower switching energies. The total half bridge switching loss for each PWM switching cycle W_{sw} is obtained by adding the appropriate column of losses from Table 1, and the average switching power loss P_{sw} is dependent on the PWM switching frequency f_{sw}:

$$P_{sw=}W_{sw}f_{sw} \tag{8}$$

The switch conduction energy loss for each PWM switching cycle W_c is determined by the voltage across the active switch, the current through the active switch, and the time of each steady state part of the PWM cycle. For example, when load current is positive, the upper switch is active for part of the PWM cycle, and the lower flyback diode is the active component for the other part of the PWM cycle. In general, a switch will be conducting for part of the PWM cycle and a diode for the other part so that the total conduction energy loss per PWM cycle is:

$$W_c = V_{ds,on} I_d t_{on} + V_{diode} I_{diode} t_{off}, \quad (9)$$

where t_{on} and t_{off} are the time the SiC MOSFET and diode, respectively, are in steady state conducting. The terms $V_{ds,on}$ and V_{diode} are the on state voltage drops across the conducting SiC MOSFET and flyback diode, respectively. Their values for the devices used in the simulations are a function of current, and are given in Table 2.

Table 2. SiC MOSFET and Flyback Diode Conducting Voltages

	I_{load}=50 A	I_{load}=40A	I_{load}=30A	I_{load}=20A	I_{load}=10A
$V_{ds,on}$ (V)	1.5	1.2	0.87	0.57	0.28
V_{diode} (V)	1.12	1	0.86	0.57	0.28

The average conduction power loss is then given by:

$$P_c = W_c f_{sw} \ . \quad (10)$$

The length of time in the conduction on and off states (t_{on} and t_{off}) for any switching device can easily be determined by the PWM cycle time ($t_{sw} = 1/f_{sw}$), the total time per PWM cycle for which the switches are in transition (i.e., the times for which there are switching losses, such as shown in Fig. 12), and the PWM duty cycle *D*. As shown in Figure 12, for example, the upper switch is in transition for approximately 50 ns during turn on, and 50 ns during turn off.

Efficiency of Half-Bridge

The efficiency of the half bridge is now analyzed over the range of load currents and for PWM switching frequencies of 20 kHz, 50 kHz, 200 kHz, and 500 kHz. It should be noted that commercially available motor drives using silicon-based switching devices tend to use PWM switching frequencies of about 25 kHz or lower to keep switching losses to a minimum and achieve good efficiency.

For consistency, the tests are each conducted with a PWM duty cycle of 50%, the load is a constant current source equal to the load current, and the SiC MOSFET is operating with a case temperature of 25 degrees C. The power output of the half bridge is obtained from the output voltage (V_{ds} of the lower switch) and the load current, while the input power is the output power plus any switching and conducting losses in both the upper and lower switch. Results of the tests, as shown in Fig. 14, demonstrate that efficiencies above 99% are possible at both 20 kHz and 50 kHz PWM switching frequencies. At the higher PWM switching frequency of 200 kHz, the switching losses begin to limit efficiency to the 96% and 97% range. Finally, at 500 kHz, the achievable efficiency begins to drop significantly to below 94%, since the switching losses begin to dominate.

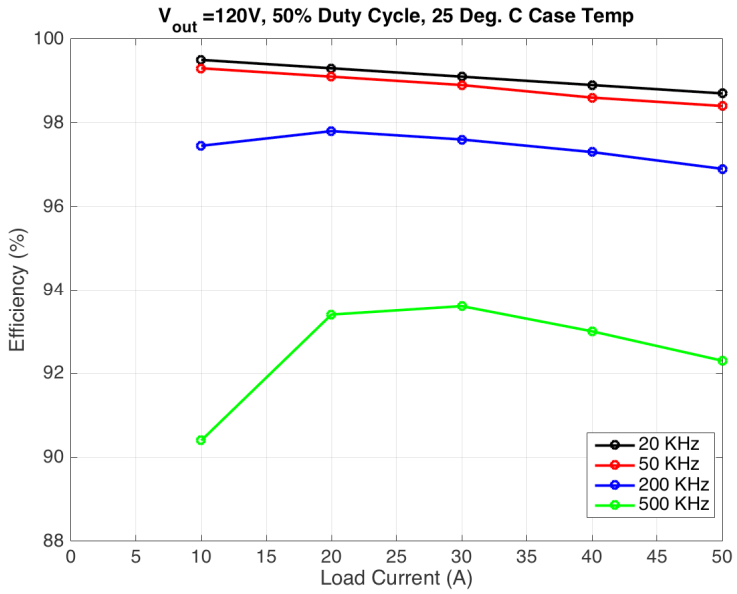


Figure 14. Half bridge efficiency versus load current for several PWM frequencies

Conclusion

The design of a SiC MOSFET half-bridge converter is presented, with emphasis on the effects of the gate drive on overall converter performance. The trade-offs between overshoot and ringing in the output, switching loss, and managing deviations in the gate-to-source voltage due to the Miller Effect and crosstalk are carefully considered to choose the gate drive components. Simulations are then performed on the half bridge to analyze the switching and conduction losses in the converter, and to determine the conversion efficiency. The results show that efficiencies of over 99% are achievable at PWM switching frequencies of 20 kHz and 50 kHz, while 97% efficiency can be reached at 200 kHz. Efficiencies of silicon IGBT and MOSFETs can also reach 99%, but only at relatively low PWM frequencies. The advantages of SiC devices can be leveraged in one of several ways. One option to operate the SiC converter at relatively low PWM frequency (20 or 50 kHz) at a higher efficiency than silicon-based switches can achieve. Another option is to operate at high PWM frequency (200 kHz, for example) and operating at efficiencies comparable to silicon switches operating at much lower PWM frequency. The higher operating frequency will allow smaller components to be used in the system to increase overall converter power density.

References

[1] Vobecky, J. (2013). The Current Status of Power Semiconductors, *Electronics and Energetics*, 28(2), 193-203.

[2] Davis, S. (2011, February). 1200V SiC MOSFET Poised to Replace Si MOSFETs and IGBTs, *Power Electronics Technology*, 36-40. Retrieved from http://powerelectronics.com/images/SiliconCarbide211.pdf

[3] Stefanskyi, A., Starzak, L., & Napieralski, A. (2015). Silicon Carbide Power Electronics for Electric Vehicles, *2015 Tenth International Conference on Ecological Vehicles and Renewable Energies*, (pp. 1-9). Monte-Carlo, Monaco.

[4] Kondrath, N., & Kazimierczuk, M.K. (2010). Characteristics and Applications of Silicon Carbide Power Devices in Power Electronics, *International Journal of Electronics and Telecommunications*, 56(3), 231-236.

[5] Ryu, S., Krishnaswami, S., Das, M., Richmond, J., Agarwal, A., Palmour, J., & Scofield, J. (2004). 2 KV 4H-SiC DMOSFETS For Low Loss, High Frequency Switching Applications, *International Journal of High Speed Electronics and Systems*, 14(3), 255-259.

[6] Colmenares, J., Peftitsis, D., Rabkowski, J., Sadik, D., Tolstoy, G., & Nee, H. (2015). High-Efficiency 312-kVA Three-Phase Inverter Using Parallel Connection of Silicon Carbide MOSFET Power Modules, *IEEE Transactions on Ind. App.*, 51(6), 4664-4676.

[7] Maswood, A.I., Benbrahim, L., & Harikrishnaraj, P., (2016). An Investigation into the Efficiency of Silicon Carbide Based Power Inverters, *2016 4th International Conference on the Developments in Renewable Energy Technology*, (pp. 1-6). Dhaka, Bangladesh.

[8] Wang, G., Wang, F., Magai, G., Lei, Y., Huang, A., & Das, M. (2013). Performance Comparison of 1200V 100A SiC MOSFET and 1200V 100A Silicon IGBT, *2013 IEEE Energy Conversion Congress and Exposition (ECCE)*, (pp. 3230-3234). Denver, Colorado.

[9] Rabkowski, J., Peftitsis, D., & Nee, H.P. (2013). Design Steps Towards a 40-kVA SiC JFET Inverter with Natural-Convection Cooling and an Efficiency Exceeding 99.5 %, *IEEE Trans Ind Appl.*, 49(4), 1589-1598.

[10] Novak, M., Novak, J., & Sivkov, O. (2015). An SiC Inverter for High Speed Permanent Magnet Synchronous Machines , IECON2015-Yokohama November 9-12, 2015. Pp. 2397-2402

[11] Batzel, T.D., & Adams, K. (2013). Variable Timing Control for ARCP Voltage Source Inverters Operating at Low DC Voltage, *International Journal of Modern Engineering (IJME)*, 13(2), 1-8.

[12] Lemmon, A., Mazzola, M.S., Gafford, J., & Parker, C. (2013). Stability Considerations for Silicon Carbide Field-Effect Transistors, *IEEE Trans. Power Electronics*, 28(10), 4453–4459.

[13] Han, D., & Sarlioglu, B. (2015). Study of the Switching Performance and EMI Signature of SiC MOSFETs Under the Influence of Parasitic Inductance in an Automotive DC-DC Converter, *2015 IEEE Transportation Electrification Conference and Expo*, (pp. 1-8), Detroit, Michigan.

[14] Chen, H., & Divan, D. (2015). High Speed Switching Issues of High Power Rated Silicon-Carbide Devices and the Mitigation Methods, *IEEE Energy Conversion Congress and Exposition*, (pp. 2254-2260), Montreal.

Biographies

TODD BATZEL received the B.S. and Ph.D. degrees in electrical engineering from the Pennsylvania State University, University Park, in 1984 and 2000, respectively, and the M.S. degree in electrical engineering from the University of Pittsburgh, Pittsburgh, PA, in 1989. Currently, he is a Professor of Electrical Engineering at Penn State University, Altoona College. Dr. Batzel may be reached at tdb120@psu.edu.

TAYLOR LEACH is presently an undergraduate student in the B.S. in electro-mechanical engineering technology (BSEMET) at Penn State Altoona, Altoona, PA. He may be reached at trl5162@psu.edu.